## AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior listing of claims:

Claims 1-16 (withdrawn)

Claim 17 (currently amended): A multi-layer printed circuit board having at least one ~~prefabricated~~ integrated electronic component comprising a circuit board substrate having a first substrate surface and a second substrate surface; a first integrated electronic component secured to the first substrate surface; where said first integrated electronic component is a prefabricated component; a first dielectric layer disposed on the first substrate surface and over the first integrated electronic component; a metallic layer disposed on the first dielectric layer; at ~~lease~~ least one via passing through the first dielectric layer and having a metal lining in contact with said metallic layer; and a second dielectric layer disposed over said via and over said metallic layer, said first dielectric layer and said second dielectric layer having a structure defining at least one opening exposing at least part of the first integrated electronic component, said opening supporting an opening metal lining which is coupled to the first integrated electronic component.

Claim 18 (original): The multi-layer printed circuit board of Claim 17 additionally comprising a first metallic layer disposed on the said first substrate surface and a second metallic layer disposed on said second substrate surface.

Claim 19 (original): The multilayer printed circuit board of Claim 17 wherein said circuit board substrate comprises a multi-layer core substrate.

Claim 20 (original): The multilayer printed circuit board of Claim 17 wherein said at least one via passes from said first substrate surface to said second substrate surface.

Claim 21 (original): The multilayer printed circuit board of Claim 18 wherein said at least one via passes from said first substrate surface to said second substrate surface.

Claim 22 (original): The multilayer printed circuit board of Claim 18 wherein said first metallic layer comprises a patterned first metallic layer to expose at least a portion of said first substrate surface, said first integrated electronic component being secured to said exposed portion of said first substrate surface.

Claim 23 (original): The multilayer printed circuit board of Claim 18 wherein said second metallic layer comprises a patterned second metallic layer to expose at least a portion of said second substrate surface.

Claim 24 ( riginal): The multilayer printed circuit board of Claim 23 additionally comprising a second integrated electronic component secured to said exposed portion of said second substrate surface.

Claim 25 (original): The multilayer printed circuit board of Claim 23 wherein said exposed portion of said second substrate surface includes a cavity.

Claim 26 (original): The multilayer printed circuit board of Claim 25 additionally comprising a second integrated electronic component disposed in said cavity.

Claim 27 (original): The multilayer printed circuit board of Claim 17 additionally comprising at least one first pad disposed on said first integrated electronic component and contacting said metallic layer.

Claim 28 (original): The multilayer printed circuit board of Claim 25 additionally comprising at least one first pad disposed on said first integrated electronic component and contacting said metallic layer.

Claim 29 (original): The multilayer printed circuit board of Claim 26 additionally comprising at least one first pad disposed on said first integrated electronic component and contacting said metallic layer.

Claim 30 (original): The multilayer printed circuit board of Claim 17 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 31 (original): The multilayer printed circuit board of Claim 25 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 32 (original): The multilayer printed circuit board of Claim 26 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 33 (original): The multilayer printed circuit board of Claim 27 additionally comprising at least one metal-lined via extending through said metallic layer and through said first dielectric layer.

Claim 34 (original): The multilayer printed circuit board of Claim 33 additionally comprising a patterned metal layer disposed n said second dielectric layer.

Claim 35 (withdrawn)